In the Claims

| 1 | 1. (currently amended) A monolithic microwave integrated circuit, comprising: |
|---|---|
| 2 | an amplifier circuit having a group delay variation verses frequency characteristic; |
| 3 | and |
| 4 | a group delay equalizer circuit integrated with said amplifier circuit to |
| 5 | compensate for said group delay variation verses frequency characteristic of said amplifier |
| 6 | circuit to frequencies above 50 GHz. |
| | |
| 1 | 2. (original) The circuit of Claim 1, wherein said amplifier circuit is capable of receiving |
| 2 | an input signal having a frequency range, amplifying said input signal and producing an output |
| 3 | signal corresponding to said amplified input signal, said group delay equalizer circuit being |
| 4 | further capable of maintaining near constant group delay of frequencies within said frequency |
| 5 | range of said input signal to prevent distortion of said output signal |
| | |
| 1 | 3. (original) The circuit of Claim 1, wherein said group delay equalizer circuit |
| 2 | comprises between 3 and 20 percent of the area of said monolithic microwave integrated circuit. |
| | |
| 1 | 4. (canceled) |
| | |
| 1 | 5. (original) The circuit of Claim 1, wherein said amplifier circuit is a distributed |
| 2 | amplifier circuit. |

| 1 | 6. (original) The circuit of Claim 5, wherein said distributed amplifier circuit comprises |
|---|--|
| 2 | one or more stages, each of said one or more stages including a common source field-effect |
| 3 | transistor, a bipolar transistor or a cascode field-effect transistor structure. |
| | |
| 1 | 7. (original) The circuit of Claim 1, wherein said amplifier circuit is a feedback |
| 2 | amplifier circuit. |
| | |
| 1 | 8. (original) The circuit of Claim 1, wherein said group delay equalizer circuit |
| 2 | comprises one or more sections, each of said sections having a different group delay response. |
| | |
| 1 | 9. (original) The circuit of Claim 8, wherein at least one of said one or more sections is |
| 2 | placed at the input of said amplifier circuit. |
| | |
| 1 | 10. (original) The circuit of Claim 8, wherein at least one of said one or more sections is |
| 2 | placed at the output of said amplifier circuit. |
| | |
| 1 | 11. (original) The circuit of Claim 8, wherein at least one of said one or more sections is |
| 2 | placed between one or more stages of said amplifier circuit. |
| | |
| 1 | 12. (original) The circuit of Claim 8, wherein said one or more sections are cascaded |
| 2 | together to form a composite group delay response capable of compensating for said group delay |
| 3 | variation verses frequency characteristic of said amplifier circuit. |

| 1 | 13. (original) The circuit of Claim 8, wherein at least one of said one or more sections |
|---|--|
| 2 | has least one microstrip line inductive over a specific frequency range and at least one capacitor |
| 3 | to create a specific phase response over at least a portion of the frequency range of said amplifier |
| 4 | circuit. |
| | |
| 1 | 14. (original) The circuit of Claim 13, wherein at least one of said one or more sections |
| 2 | is a filter selected from the group consisting of: an LC filter, a bridged LC filter, an RC filter and |
| 3 | an RLC filter. |
| | |
| 1 | 15. (original) The circuit of Claim 13, wherein at least one of said one or more sections |
| 2 | is a filter with a microstrip transformer. |
| | |
| 1 | 16. (original) The circuit of Claim 1, further comprising: |
| 2 | a substrate, said amplifier circuit and said group delay equalizer circuit being |
| 3 | fabricated in said substrate. |
| | |
| 1 | 17. (original) The circuit of Claim 16, wherein said substrate is made from a material |
| 2 | selected from the group consisting of: a III-V material, a II-VI material and a heterostructure |
| 3 | material. |
| | |
| 1 | 18. (original) The circuit of Claim 1, wherein said group delay equalizer circuit is |
| 2 | further capable of allowing a near constant gain response to be achieved over the frequency |
| 3 | range of said amplifier circuit. |

| I | 19. (currently amended) A method for providing a near constant group delay over a |
|---|---|
| 2 | frequency range of a amplifier circuit, comprising the steps of: |
| 3 | providing said amplifier circuit within a monolithic microwave integrated circuit, |
| 4 | said amplifier circuit having a group delay response variation verses frequency characteristic; |
| 5 | and |
| 6 | integrating a group delay equalizer circuit with said amplifier circuit on said |
| 7 | monolithic microwave integrated circuit to compensate for said group delay variation verses |
| 8 | frequency characteristic of said amplifier circuit to frequencies above 50 GHz. |
| | |
| 1 | 20. (original) The method of Claim 19, further comprising the steps of: |
| 2 | receiving an input signal having a frequency range at said amplifier circuit; |
| 3 | amplifying said input signal to produce an output signal corresponding to said |
| 4 | amplified input signal; and |
| 5 | maintaining, by said group delay equalizer circuit, near constant group delay of |
| 6 | frequencies within said frequency range of said input signal to prevent distortion of said output |
| 7 | signal. |
| | |
| 1 | 21. (original) The method of Claim 19, wherein said group delay equalizer circuit |
| 2 | comprises between 3 and 20 percent of the area of said monolithic microwave integrated circuit. |
| | |
| 1 | 22. (canceled) |

| 1 | 23. (original) The method of Claim 19, wherein said step of integrating further |
|---|---|
| 2 | comprises the step of: |
| 3 | integrating one or more sections of said group delay equalizer circuit with said |
| 4 | amplifier circuit on said monolithic microwave integrated circuit, each of said sections having a |
| 5 | different group delay response. |
| | |
| 1 | 24. (original) The method of Claim 23, wherein said step of integrating said one or more |
| 2 | sections further comprises the step of: |
| 3 | placing at least one of said one or more sections at the input of said amplifier |
| 4 | circuit. |
| | |
| 1 | 25. (original) The method of Claim 23, wherein said step of integrating said one or more |
| 2 | sections further comprises the step of: |
| 3 | placing at least one of said one or more sections at the output of said amplifier |
| 4 | circuit. |
| | |
| 1 | 26. (original) The method of Claim 23, wherein said step of integrating said one or more |
| 2 | sections further comprises the step of: |
| 3 | placing at least one of said one or more sections between one or more stages of |
| 4 | said amplifier circuit. |
| | |
| 1 | 27. (original) The method of Claim 23, wherein said step of integrating said one or more |
| 2 | sections further comprises the step of: |

cascading said one or more sections together to form a composite group delay 3 response capable of compensating for said group delay variation verses frequency characteristic 4 5 of said amplifier circuit. The method of Claim 19, wherein said step of integrating further 1 28. (original) comprises the step of: 2 integrating said group delay equalizer circuit with said amplifier circuit on said 3 monolithic microwave integrated circuit to allow a near constant gain response to be achieved 4 over the frequency range of said amplifier circuit. 5 29. (new) A monolithic microwave integrated circuit, comprising: 1 an amplifier circuit having a group delay variation verses frequency characteristic; 2 3 and a group delay equalizer circuit integrated with said amplifier circuit to 4 compensate for said group delay variation verses frequency characteristic of said amplifier 5 circuit, said group delay equalizer circuit comprising a plurality sections, each section having a 6 different group delay response, said plurality of sections being cascaded to form an overall 7 composite group delay response. 8 30. (new) The monolithic microwave integrated circuit of claim 29, wherein said 1

2

amplifier circuit has a plurality of stages.

- 1 31. (new) The monolithic microwave integrated circuit of claim 30, wherein said 2 plurality of sections can be separated by said plurality of stages.
- 1 32. (new) The monolithic microwave integrated circuit of claim 29, wherein said
- 2 group delay equalizer circuit is capable of compensating for said group delay variation verses
- 3 frequency characteristic of said amplifier circuit to frequencies above 50 GHz.